REMARKS

Claims 1-50 are pending. As discussed below, claims 1-50 are now in condition for allowance. Furthermore, although the Examiner indicates on the second page of the Office Action that claim 50 is rejected, she provides no reason for rejection. Moreover, because the patent application discloses and claims relatively complex subject matter, the Applicant's attorney believes that he and the Examiner may facilitate prosecution of this application by discussing it over the phone. Therefore, per the voice mail that the Applicant's attorney left for the Examiner on May 11, 2005, the Applicant's attorney requests a teleconference with the Examiner regarding the application if the Examiner does not allow all of the claims after considering this response.

Amendment to the Specification

At the Examiner's suggestion, the Applicant's attorney has amended the specification to recite "first" and "second" Viterbi detectors to clarify an embodiment of the invention on which claim 36 reads. But this amendment adds no new matter to the patent application.

Rejection Of Claims 1-5 and 49 Under 35 U.S.C. § 102(e) As Being Anticipated By U.S. Patent 6,144,513 to Reed

As discussed below, the Applicant's attorney disagrees with this rejection.

Claim 1

Claim 1 recites a determinator operable to determine the connection polarity of a read-write head from recovered servo data.

For example, a read-write head 14 reads servo data from a magnetic data-storage disk 12 and generates a servo signal that includes the servo data. Read-write head 14 is coupled to servo circuit 60 with a connection polarity (head connection reversed or not reversed), and a Viterbi detector 100 recovers a sync mark from the

servo signal. A comparator 104 determines the connection polarity of read-write head 14 from the recovered sync mark. More specifically, by comparing the recovered sync mark to a stored (in register 106) noninverted copy of the sync mark, comparator 104 can determine the connection polarity of read-write head 14. If comparator 104 determines that the head connection is reversed, then the comparator can generate a signal that causes a phase-compensation circuit 64 to compensate for this reversed connection. If comparator 104 determines that the head connection is not reversed, then no compensation is needed.

In contrast, Reed neither discloses nor suggests a determinator operable to determine the connection polarity of a read-write head from the recovered servo data. Instead, Reed simply discloses a pulse detection circuit for indicating the *presence of pulses* in a servo signal (col. 4, lines 54-67 and col. 11, lines 12-67). Specifically, a pulse is detected only if its polarity is opposite in sign from the polarity of the previous pulse (col.4, lines 63-64 and col.11, lines 54-67). Reed defines the "polarity" of a pulse as either positive or negative, such that a pulse is only detected if it exceeds a positive or negative threshold for a positive or negative peak, respectively (Fig. 8 and col. 11, lines 12-41). By simply measuring whether the peak, or amplitude, of a pulse exceeds a given threshold and whether it is opposite in direction to the previous peak, Reed's pulse detection circuit is less susceptible to noise (col. 4, lines 64-67). This has nothing to do with determining the connection polarity of a read-write head.

Claims 2-5

These claims are patentable by virtue of their dependencies from claim 1.

Claim 49

Claim 49 recites sampling a servo signal having a phase, and recovering servo data from the servo signal regardless of the phase of the servo signal.

For example, as discussed above in support of the patentability of claim 1, Viterbi detector 100 recovers servo data from the servo signal, and in this example, the phase

of the servo signal corresponds to the connection polarity of a read-write head 14. Because a comparator 104 determines the phase of the servo signal and can generate a signal that causes a phase-compensation circuit 64 to compensate for an inverted phase, servo data from the servo signal is recovered regardless of the phase of the servo signal.

In contrast, Reed neither discloses nor suggests sampling a servo signal having a phase, and recovering servo data from the servo signal regardless of the phase of the servo signal. As discussed above, Reed simply discloses a pulse detection circuit for indicating the *presence of pulses* in a servo signal (col. 4, lines 54-67 and col. 11, lines 12-67). This pulse detection circuit measures whether the peak, or amplitude, of a pulse exceeds a given threshold and whether it is opposite in direction to the previous peak. This has nothing to do with recovering servo data from the servo signal regardless of the phase of the servo signal.

Rejection Of Claims 6-24, 27-41 Under 35 U.S.C. § 102(e) As Being Anticipated By U.S. Patent 6,108,151 to Tuttle

As discussed below, the Applicant's attorney disagrees with this rejection.

Claim 6

Claim 6 recites a recovery circuit operable to recover a binary sequence having pairs and only pairs or consecutive first logic levels and consecutive second logic levels, and operable to calculate a respective path metric for each of no more than two possible states of the binary sequence.

For example, referring to FIG. 7C of the patent application, the Viterbi detector 100 calculates a respective path metric for each of no more than two possible states — here S0 and S3 — of a binary sequence having pairs and only pairs of consecutive first logic levels and consecutive second logic levels. That is, the Viterbi detector 100 calculates respective path metrics for the possible states S0 and S3, but calculates no path metrics for the possible states S1 and S2. It should be emphasized that the

possible states have *pairs and only pairs* of consecutive logic levels, for example 00 and 11. By definition, it necessarily follows that Viterbi detector 100 must be a duobinary detector (for example a PR4 detector) and not a dicode detector. The possible states of a dicode detector only have a single logic digit, for example 0 and 1. Viterbi detector 100 is unique in that it is a duobinary detector *and* calculates a respective path metric for no more than two possible states.

In contrast, although Tuttle discloses a binary sequence having pairs and only pairs or consecutive first logic levels and consecutive second logic levels, he fails to disclose recovering the sequence by calculating a respective path metric for each of no more than two possible states of the binary sequence.

Claims 7-12

These claims are patentable by virtue of their dependencies from claim 6.

Claim 13

Claim 13 recites a recovery circuit operable, for each pair of samples of a signal that represents a binary sequence having pairs and only pairs of consecutive logic 0's and logic 1's, to calculate multiple path metrics for no more than two possible states of the binary sequence.

In contrast, although Tuttle discloses a binary sequence having pairs and only pairs or consecutive first logic levels and consecutive second logic levels, he fails to disclose, for each pair of samples of a signal that represents the binary sequence, calculating a respective path metric for each of no more than two possible states of the binary sequence.

Claims 14-16

These claims are patentable by virtue of their dependencies from claim 13.

Claim 17

Claim 17 recites a recovery circuit that, for each pair of samples of a signal that represents a binary sequence having pairs and only pairs of consecutive logic 0's and logic 1's, is operable to calculate a difference between path metrics for two possible states of the binary sequence and to determine a surviving path from the difference.

In contrast, although Tuttle discloses a binary sequence having pairs and only pairs or consecutive logic 0's and logic 1's, he fails to disclose, for each pair of samples of a signal that represents the binary sequence, calculating a differrence between path metrics for two possible states of the binary sequence and to determine a surviving path from the difference.

Claims 18-20

These claims are patentable by virtue of their dependencies from claim 17.

Claim 21

Claim 21 recites a comparator operable to determine the connection polarity of a read head from the recovered synchronization mark.

Claim 21 is patentable over Tuttle for reasons similar to those recited above in support of the patentability of claim 1 over Reed. Specifically, col 19, line 22 – col. 20, line 22 of Tuttle is a virtually verbatim copy of Reed's col. 11, line 12 – col. 12, line 10 (note that these two patents have a common assignee and some common inventors). Therefore, the reasons recited above in support of the patentability of claim 1 over Reed also support the patentability of claim 21 over Tuttle.

Claims 22-24

These claims are patentable by virtue of their dependencies from claim 21.

Claim 27

Claim 27 recites a comparator operable to determine the phase of a servo signal from a recovered synchronization mark.

For example, as discussed above in support of the patentability of claim 1, a comparator 104 determines the connection polarity of a read-write head 14 from a synchronization mark recovered by a Viterbi detector 100. In this example, the phase of the servo signal corresponds to the connection polarity. That is, if the connection of read-write head 14 is not reversed, then the servo signal has a noninverted phase. Conversely, if the connection of head 14 is reversed, then the servo signal has an inverted phase.

In contrast, Tuttle neither discloses nor suggests a comparator operable to determine the phase of a servo signal from a recovered synchronization mark. Instead, Tuttle simply discloses a pulse detection circuit for indicating the *presence of pulses* in a servo signal (col. 19, line 22 – col. 20, line 22). As discussed above, col 19, line 22 – col. 20, line 22 of Tuttle is a virtually verbatim copy of Reed's col. 11, line 12 – col. 12, line 10. A pulse is detected only if its peak, or amplitude, exceeds a given threshold and is opposite in sign from the peak of the previous pulse (Fig. 17 and col. 19, line 22 – col. 20, line 12). The pulse detection circuit of Tuttle only measures the amplitude and sign of individual pulses within a servo signal, and does not recover a synchronization mark from the servo signal. As a result, the circuit has nothing to do with determining the phase of the entire servo signal from a single synchronization mark.

Claims 28-32

These claims are patentable by virtue of their dependencies from claim 27.

Claim 33

Claims 33 is patentable for reasons similar to those recited above in support of the patentability of claim 27.

Claims 34-35

These claims are patentable by virtue of their dependencies from claim 33.

Claim 36

Claim 36 is patentable for reasons similar to those recited above in support of the patentability of claim 27.

Claim 37

Claim 37 recites a Viterbi detector operable to recover a synchronization mark and other servo data from samples of a servo signal regardless of the phase of the servo signal.

For example, referring to FIGS. 6-7C and paragraphs [41] – [48] of the patent application, a read-write head 14 (FIG. 1) reads a sync mark and other servo data from a magnetic storage disk 12 (FIG. 1), and generates a servo signal that includes the sync mark and other servo data. The head 14 is coupled to a Viterbi detector 100 with a connection polarity — the phase of the servo signal corresponds to the head's connection polarity — that can either be inverted (head connection reversed) or noninverted (head connection not reversed), but the detector 100 recovers the sync mark (and may also recover other servo data) from the servo signal regardless of the connnection polarity.

In contrast, Tuttle neither discloses nor suggests a Viterbi detector that recovers a synchronization mark and other servo data from samples of a servo signal regardless of the phase of the servo signal. Instead, Tuttle simply discloses a pulse detection circuit for detecting individual data pulses in a servo signal (col. 19, line 22 – col. 20, line 22). Nowhere does Tuttle disclose or suggest a *Viterbi detector* for recovering a synchronization mark and other servo data regardless of the phase of the *entire* servo signal.

Claim 38

Claim 38 recites recovering servo data from a servo signal having a phase that represents the connection polarity of a read head, and determining the phase of the servo signal from the recovered servo data.

For example, a read-write head 14 reads servo data from a magnetic data-storage disk 12 and generates a servo signal that includes the servo data. Read-write head 14 is coupled to servo circuit 60 with a connection polarity (head connection reversed or not reversed), and the servo signal has a phase that represent the connection polarity. A Viterbi detector 100 recovers the servo data from the servo signal, and a comparator 104 determines the phase of the servo signal, and thus the connection polarity of read-write head 14. More specifically, by comparing a recovered sync mark to a stored (in register 106) noninverted copy of the sync mark, comparator 104 can determine the phase of the servo signal (i.e., the connection polarity of read-write head 14). If comparator 104 determines that the phase is inverted (head connection is reversed), then the comparator can generate a signal that causes a phase-compensation circuit 64 to compensate for this inverted phase. If comparator 104 determines that the phase is noninverted (head connection is not reversed), then no compensation is needed.

In contrast, Tuttle neither discloses nor suggests recovering servo data from a servo signal having a phase that represents the connection polarity of a read head, and determining the phase of the servo signal from the recovered servo data. Instead, Tuttle simply discloses determining the *presence of pulses* in a servo signal (col. 19, line 22 – col. 20, line 22). As discussed above, col 19, line 22 – col. 20, line 22 of Tuttle is a virtually verbatim copy of Reed's col. 11, line 12 – col. 12, line 10. The method of Tuttle determines that a pulse is present in the servo signal if its peak, or amplitude, exceeds a given threshold and is opposite in sign from the peak of the previous pulse (Fig. 17 and col. 19, line 22 – col. 20, line 12). This method only sees the servo signal as a series of individual pulses, each having an amplitude and a sign. Tuttle discloses nothing about the servo data having a phase that represents a connection polarity of the

read head. Furthermore, Tuttle discloses nothing about determining the phase of the entire servo signal from the recovered servo data.

Claims 39-41

These claims are patentable by virtue of their dependencies from claim 38.

Rejection Of Claims 43-48 Under 35 U.S.C. § 102(b) As Being Anticipated By U.S. Patent 5,822,143 to Cloke

As discussed below, the Applicant's attorney disagrees with this rejection. Also, even though on page 9 the rejection of claim 43 appears to be in view of Tuttle, it seems from the rejections of claims 44-48 that the Examiner intended to reject claim 43 in view of Cloke. Therefore, the Applicant's attorney treats the rejection of claim 43 as being in view of Cloke, not Tuttle.

Claim 43

Claim 43 recites calculating a respective path metric for each of no more than two possible states of a binary sequence having pairs and only pairs of consecutive first logic levels and consecutive second logic levels.

For example, referring to FIG. 7C of the patent application, the Viterbi detector 100 calculates a respective path metric for each of no more than two possible states — here S0 and S3 — of a binary sequence having pairs and only pairs of consecutive first logic levels and consecutive second logic levels. That is, the Viterbi detector 100 calculates respective path metrics for the possible states S0 and S3, but calculates no path metrics for the possible states S1 and S2. It should be emphasized that the possible states have *pairs and only pairs* of consecutive logic levels, for example 00 and 11. By definition, it necessarily follows that Viterbi detector 100 must be a duobinary detector (for example a PR4 detector) and not a dicode detector. The possible states of a dicode detector only have a single logic digit, for example 0 and 1. Viterbi detector

100 is unique in that it is a duobinary detector *and* calculates a respective path metric for no more than two possible states.

In contrast, Cloke neither discloses nor suggests calculating a respective path metric for each of no more than two possible states of a binary sequence having pairs and only pairs of consecutive first logic levels and consecutive second logic levels. Instead, Cloke's Viterbi detector 111 calculates path metrics for each of *more than two* possible states of a binary sequence (FIGS. 1A, 1B and 1C). For example, referring to FIG. 1A, in the PR4 implementation, Cloke's Viterbi detector 111 calculates path metrics for all four possible states 00, 10, 01, 11. The Examiner attempts to argue that col. 4, lines 51-64 of Cloke teaches calculating path metrics of just two possible states. However, the Examiner correctly points out that this portion of Cloke only teaches a *dicode* detector using the polynomial P(D) where m=0 (dicode). When m=0, the polynomial P(D) is *not* duobinary, and therefore does not apply to logic states having pairs and only pairs of consecutive first logic levels and consecutive second logic levels.

Claim 44

This claim is patentable by virtue of it's dependency from claim 43.

Claims 45-46

Claim 45 is patentable for reasons similar to those recited above in support of the patentability of claim 43, and claim 46 is patentable by virtue of its dependency from claim 45.

Claim 47

Claim 47 recites sampling a signal that represents a binary sequence having pairs and only pairs of consecutive logic 0's and logic 1's, for each pair of samples, calculating a difference between path metrics for two possible states of the binary sequence, and determining a surviving path from the difference.

For example, referring to FIG. 7C and paragraphs [48] – [56] of the patent application, the Viterbi detector 100 calculates a difference between the path metrics for two possible states — here S0 and S3 — of a binary sequence having pairs and only pairs of consecutive logic 0's and logic 1's, and determines a surviving path from this calculated difference.

In contrast, Cloke neither discloses nor suggests that the Viterbi detector 111 calculates a difference between path metrics for two possible states, and determines a surviving path from the difference. In the Examiner's Response to Arguments, the Examiner uses the same argument for claims 43, 45 and 47. As a result, the reasons recited above in support of the patentability of claim 43 also apply here.

Claim 48

This claim is patentable by virtue of its dependency from claim 47.

Rejection Of Claims 25-26 and 42 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Tuttle In View Of Cloke

As discussed below, the Applicant's attorney disagrees with this rejection.

Claims 25-26

Claims 25-26 are patentable by virtue of their dependencies from independent claim 21.

Claim 42

Claim 42 is patentable by virtue of its dependency from independent claim 38.

Rejection Of Claim 34 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Tuttle In View Of U.S. Patent 6,490,110 To Reed

Claim 34 is patentable by virtue of its dependency from independent claim 33.

CONCLUSION

In view of the foregoing, the Applicant's attorney believes that claims 1-50 as previously pending are in condition for allowance. Consequently, the issuance of a formal Notice of Allowance at an early date is respectfully requested.

As discussed above, the Applicant's attorney requests that if the Examiner still believes that not all of the claims are allowable, she contact the Applicant's attorney at (425)-455-5575 to schedule a phone interview.

Respectfully submitted,

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